Introduction

NEED FOR FULL ELECTROMAGNETIC VERIFICATION.

Electromagnetic (EM) and Integrated Circuits (IC) designers are working nowadays on large circuits that contain different IPs on the same chip, and they crucially need to apply full electromagnetic extraction to perform verification analyses. During such verification phase, it is crucial to study effects such as delay, energy consumption, capacitive crosstalk, and inductive coupling. However, modeling the full EM effects for many IPs on the same chip results in a parasitics explosion and massive circuits containing billions of elements and nodes, which is a critical challenge during the verification stage.

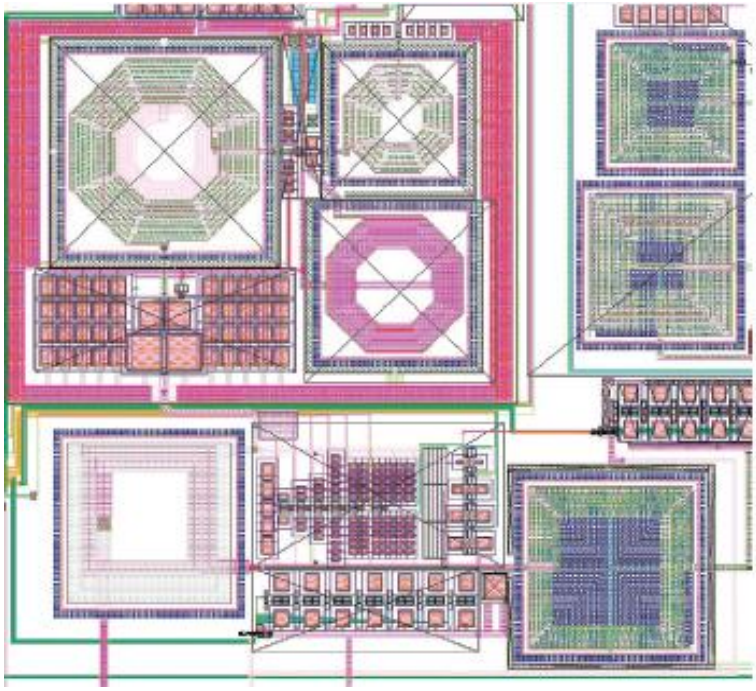

Figure 1 Analog RF block containing numerous interconnects. Ref [ANSYS-RaptorX-Data-Sheet]

BOTTLENECK WITH SIMULATION TIME.

The aforementioned parasitics explosion causes verification analyses to be very slow, so designers tend to trade extraction of full EM to do verification analyses before fabrication. However, the industry tends to increase developing chips to support 5G and with the increasing number of high performance modules (e.g. SERDES see Figure2) in their chips; therefore, it becomes mandatory to study the full EM effects and develop new techniques to facilitate full-chip verification analyses.

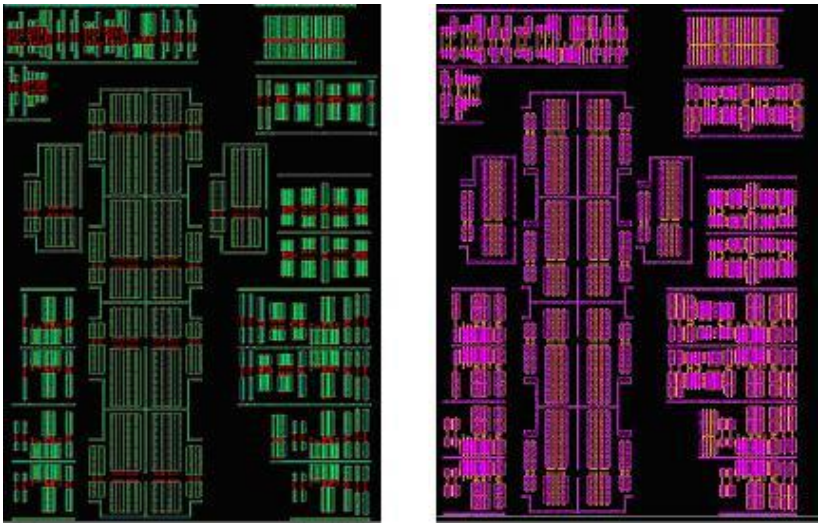

Figure 2 SerDes Layout of 65nm (green) and 45nm (purple).
Ref[https://semiwiki.com/uncategorized/559-65nm-to-45nm-serdes-ip-migration-success-story/]

MOREAL IS SUPERIOR.

MOReal, a state-of-the-art model order reduction tool, provides a seamless solution that can be implemented in both digital and analog flows. MOReal reduces large circuits rapidly to a small realizable circuit ready for simulation. The reduced circuits maintain the behavior of the original netlists and, most importantly, perform the necessary analyses and simulations very quickly. MOReal also has a guaranteed passive and numerically stable algorithm. It can grasp many ports as well as producing a realizable RLCK circuit.

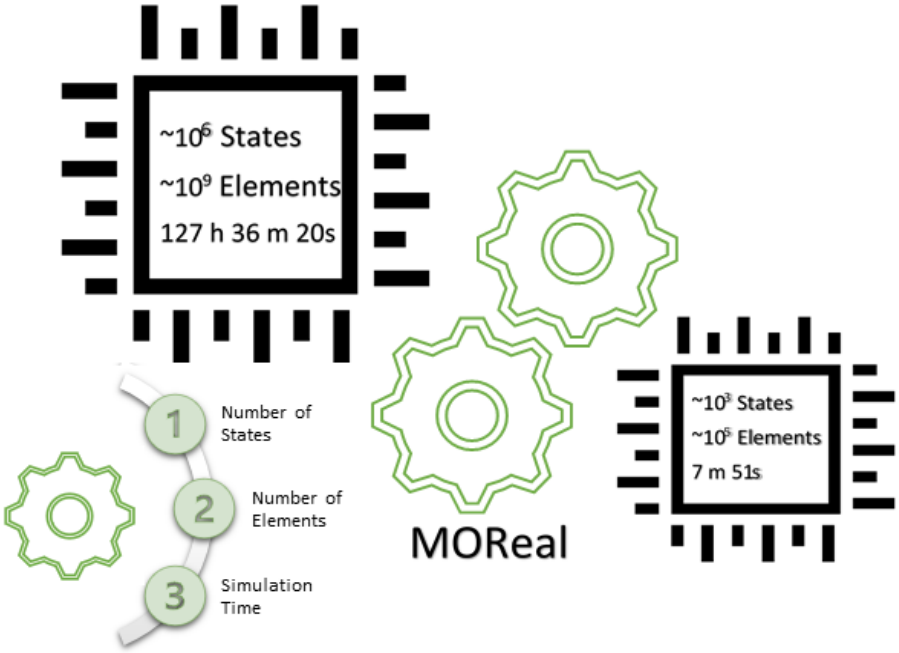

Figure 3 MOReal reduces Number of nodes and elements enhancing simulation time

Capabilities of MOReal with Digital and Analog Flows

MOReal is compatible with both analog and digital flows. It is prepared to reduce circuits produced by industrial extraction tools such as Quantus, Clarity, Calibre, Ansys VeloceRF, Ansys RaptorX, and StarRC, and It supports different circuit formats (SPICE, SPECTRE, SPEF) that represent both analog and digital circuits.

Analog and Digital Test Cases

Analog and digital circuits consist of either RC, RCC, RLC, RLCK elements. MOReal can automatically detect the type of the extracted netlist and returns to the user a reduced netlist consists only of the same components used for extraction without adding non-physical sources. Table 1 gives a summary of the results of some challenging RLCK industrial test cases, as shown in Figure 4, an RCC test case of voltage-controlled-oscillator (VCO), and an RC Digital IP circuit. One of the most remarkable advantages of MOReal is that reducing circuits with hundreds of ports very quickly in a range of seconds.

Table 1 Reduction Results of Analog and Digital Circuits

Circuit ID.	Circuit Type	No. Ports	NO. states	Reduction	Reduction time (s)
Analog IP1	RLCK	23	13,811 → 340	40.6X	2.19
Analog IP2	RLCK	8	16,502 →264	62.5X	8.38
Analog IP3	RLCK	6	28,716 → 181	158.7X	22.6
Analog IP4	RLCK	101	56,434 → 1,382	40.8X	148.46
Analog IP5	RCC	565	12,671→ 565	22X	3.1
Digital IP6	RC	380,728	1,568,602 → 380,728	4X	342

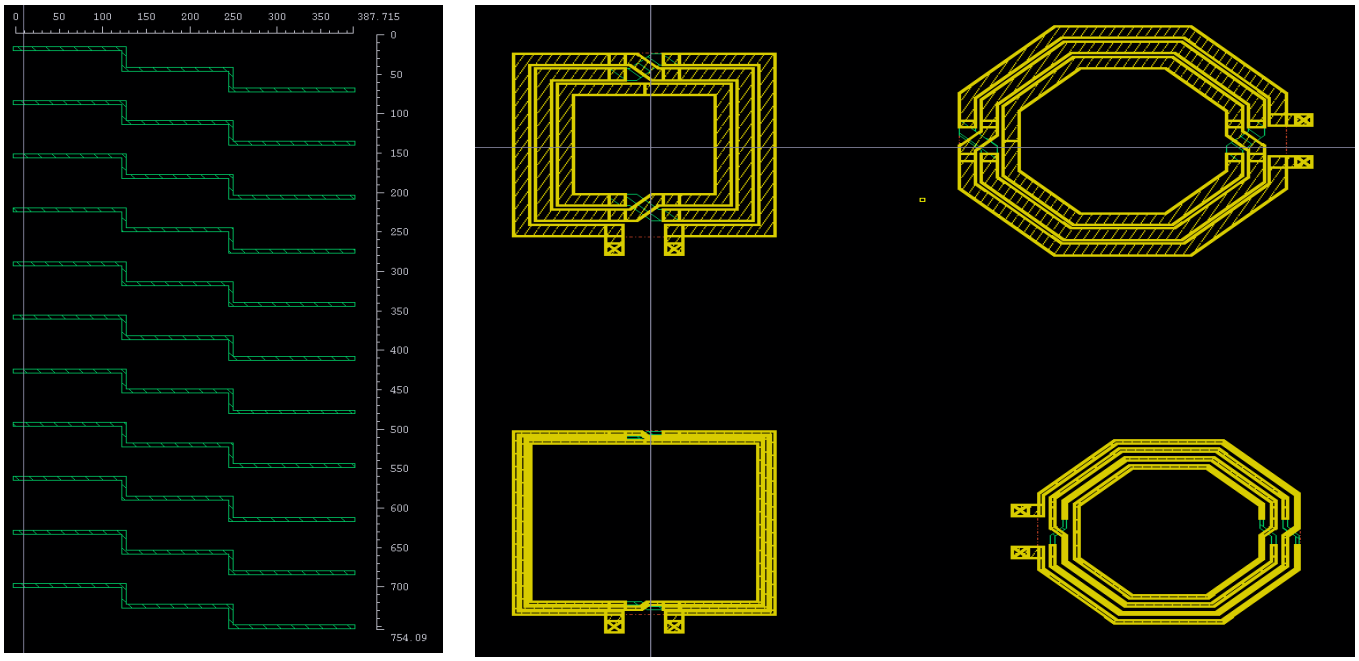

Figure 4 Layout (Visualization) of the bus and four inductors testcases.

Different Reduction Modes in MOReal

Most of the physical extraction tools produce parasitic circuits modeling the interconnect's behavior along a **wideband** of frequencies, which is from DC up to a higher frequency. On the other hand, some physical extractors can model these interconnects around a single frequency point because the users are interested in working around this point, excluding other frequencies, so they support the **narrowband** approach. MOReal supports two modes of reduction:

- **Wideband**

In this mode, MOReal's reduction process guarantees the accuracy from DC up to the selected frequency as described in Figure 5. Table 2 summarizes the remarkable results obtained from MOReal's wideband reduction mode after testing different RLCK industrial test cases.

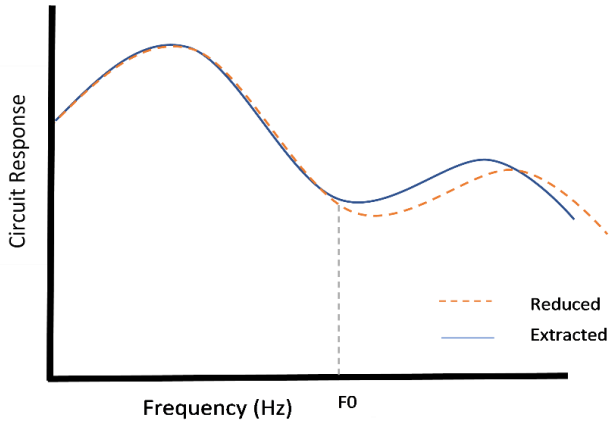

Figure 5 A figure to illustrate the wideband reduction mode

Table 2 Wide-band reduction for different IPs (DC → 50 GHz)

Circuit ID.	No. Ports	Number of States			Number of Elements			Simulation Time (SP)		
		Original	MOReal	Reduction%	Original	MOReal	Reduction%	Original	MOReal	Speedup
1	6	28,716	181	159X	29,459,890	10,977	2684X	NA	260.9 ms	∞
2	3	20,371	104	196X	24,097,020	3,645	6611X	NA	72.7 ms	∞
3	8	16,502	264	63X	10,875,177	21,238	512X	NA	1.37 s	∞
4	101	56,434	1,382	41X	139,988,870	633,608	221X	NA	1m 43s	∞
5	7	16,266	147	111X	8,169,040	7,355	1111X	NA	146.9 ms	∞
6	23	13,811	340	41X	7,466,401	40,731	183X	NA	1.38 s	∞
7	38	9,277	447	21X	4,145,116	77,597	53X	NA	21.8 s	∞
8	2	3,672	59	62X	10,805,601	1,148	9413X	35m3.8s	20.6 ms	**60,000X**

- **Narrowband**

Some extraction tools produce narrowband parasitic netlists that model the circuits at a single frequency; therefore, applying a wideband approach to them may result in an unnecessarily large reduced circuit.

The narrowband mode guarantees the accuracy at this frequency, as shown in Figure 6, while producing much fewer nodes and elements than the wideband approach. Table 3 shows the results of the same previous RLCK test cases after applying MOReal's narrowband reduction.

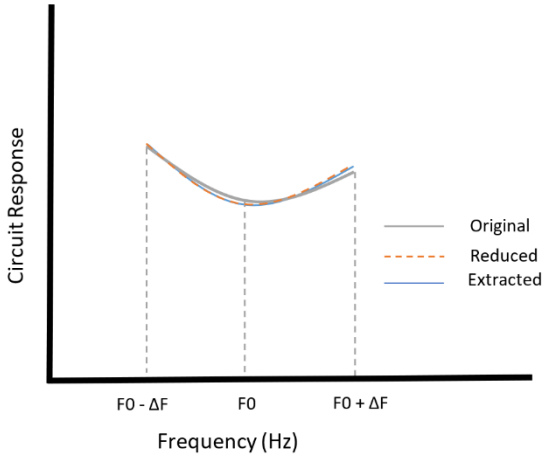

Figure 6 An illustration of the narrow-band reduction mode.

Table 3 Narrowband Reduction (At 50 GHz)

Circuit ID.	No. Ports	Number of States			Number of Elements			Simulation Time (SP)		
		Original	MOReal	Reduction%	Original	MOReal	Reduction%	Original	MOReal	Speedup
1	6	28,716	32	897X	29,459,890	412	71505X	NA	19.366 ms	∞
2	3	20,371	15	1358X	24,097,020	95	253653X	NA	12.147 ms	∞
3	8	16,502	40	413X	10,875,177	578	18815X	NA	22.488 ms	∞
4	101	56,434	501	113X	139,988,870	87,042	1608X	NA	3.50 s	∞
5	7	16,266	33	493X	8,169,040	448	18234X	NA	20.265 ms	∞
6	23	13,811	115	120X	7,466,401	4,461	1674X	NA	224.032 ms	∞
7	38	9,277	171	54X	4,145,116	11,962	347X	NA	1.9 s	∞
8	2	3,672	10	367X	10,805,601	46	234904X	35m3.8s	11.519 ms	**120,000X**

Comparison between Wideband and Narrowband Reduction

Table 4 displays the gain in reduction and simulation time when choosing the narrowband over the wideband mode in the same RLCK examples reported in Table 4. Table 5 also shows the significant changes in file sizes after applying narrowband and wideband reduction compared to the size of the extracted file.

Therefore, selecting the narrowband mode when it is possible by design is significantly rewarding because it produces a higher reduction ratio and enhances the simulation time of the circuit.

Table 4 Comparison between wideband and narrowband modes.

Circuit ID	Wide Band			Narrow Band @ 50 GHz		
	#States	#Elements	Sim-Time	#States	#Elements	Sim-Time
1	181	10,977	260.94 ms	32	412	19.366 ms
2	104	3,645	72.7 ms	15	95	12.147 ms
3	264	21,238	1.372 s	40	578	22.488 ms
4	1,382	633,608	1m 43 s	501	87,042	3.50 s
5	147	7,355	146.869 ms	33	448	20.265 ms
6	340	40,731	1.3827 s	115	4,461	224.032 ms
7	447	77,597	21.768 s	171	11,962	1.9 s
8	59	1,148	20.674 ms	10	46	11.519 ms

Table 5 Comparison of the extracted netlist and the wideband and narrowband file sizes.

Circuit ID	Extracted	Wide Band	Narrow Band
1	4.1 GB	0.459 MB	20.1 KB
2	2.1 GB	180.6 KB	3.8 K
3	1.5 GB	0.85 MB	23.1 KB
4	12.8 GB	34.6 MB	3.8 MB
5	697.9 MB	377.7 KB	17.7 KB
6	643.8 MB	2.35 MB	178.6 KB
7	365.5 MB	4.1 MB	466.7 KB
8	90.2 MB	44.65 KB	1.9 KB

MOReal improves the conditioning of reduced systems

MOReal reduces netlists and returns RLCK circuit to the user with better system conditioning. Conditioning is an important property for simulation tools since well-conditioned systems always simulate faster than bad conditioned system. MOReal is employed to help reduce parasitics networks besides applying innovative techniques to improve their conditioning, so reduced circuits speed up during verification analyses and simulations.

The graph displayed in Figure 7 studies the convergence of iterative solvers that are used in simulators and are enhanced by conditioning resulting in shorter simulation time.

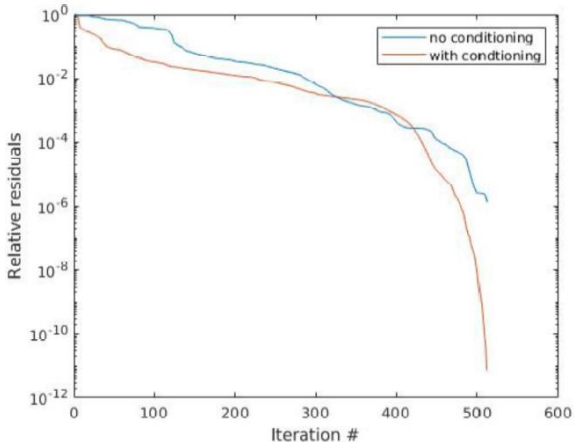

Figure 7 The graph illustrates the significant impact of MOReal on iterative solvers.

MOReal's accuracy

The reduced circuits produced by MOReal has much better accuracy than those reduced by MOR techniques found in the literature such as PRIMA. Although MOReal results in a very small circuit compared to PRIMA, MOReal still has superior accuracy over literature MOR algorithms.

The graph in Figure 8 shows an accuracy comparison between MOReal and PRIMA in S-parameters simulation.

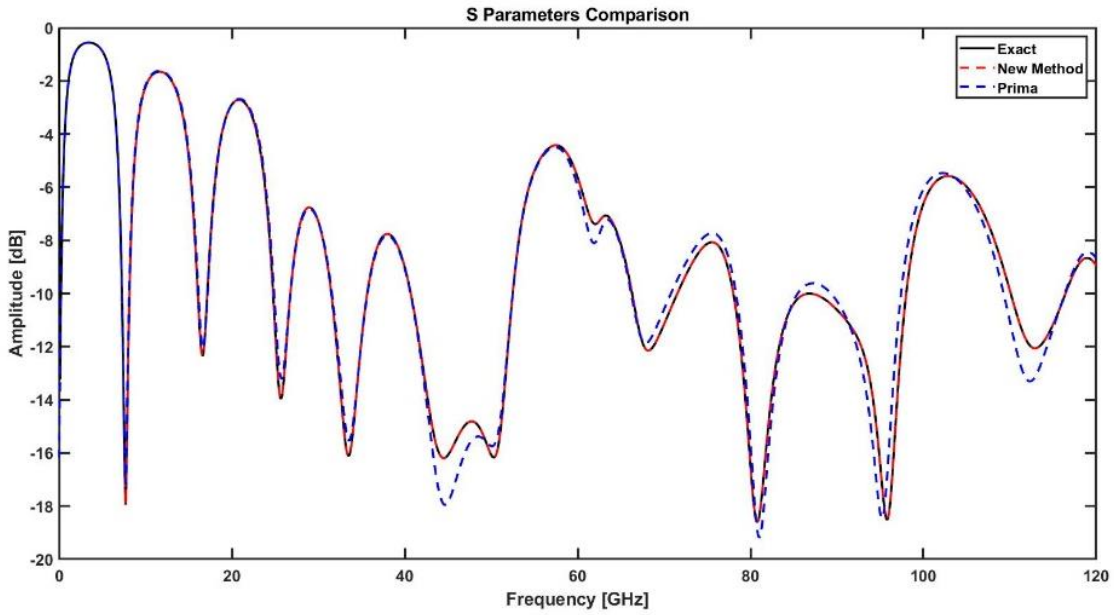

Figure 8 The graph shows how accurate MOReal is relative to the original circuit compared to PRIMA algorithm.

Output Netlists Structure

MOReal can preserve all the characteristics and properties of extracted netlists in the new reduced output circuit. Furthermore, MOReal realizes the reduced system using only physical instances only that are resistors, capacitors, inductors, and mutual inductors (R, L, C, K).

MOReal's process supports "RLCK in – RLCK out."

Figure 9 illustrates how MOReal reduces a large netlist of RLCK to RLCK small equivalent circuit.

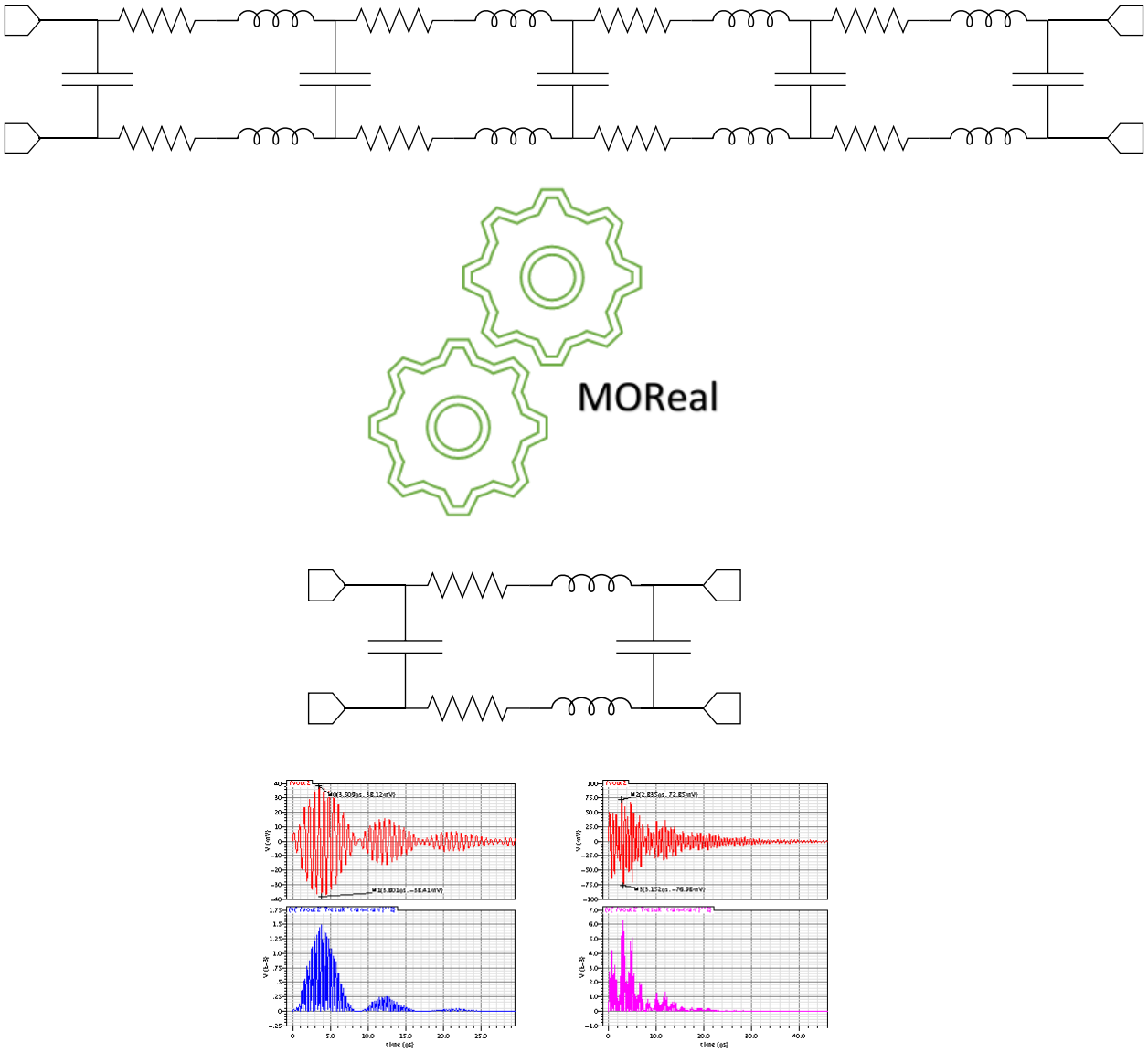

Figure 9 An Illustration of MOReal's operation. The above circuit represents a large extracted circuit (original), and the second below picture represent a reduced RLCK circuit with less parasitic instances

MOReal also has this unique ability to preserve all properties of an RLCK netlist and reduce it to an equivalent RC circuit. The RC circuit is a mathematical equivalent system that is equivalent to the original circuit.

MOReal's supports "RLCK in – RC out."

Figure 10 illustrates the equivalent RC network.

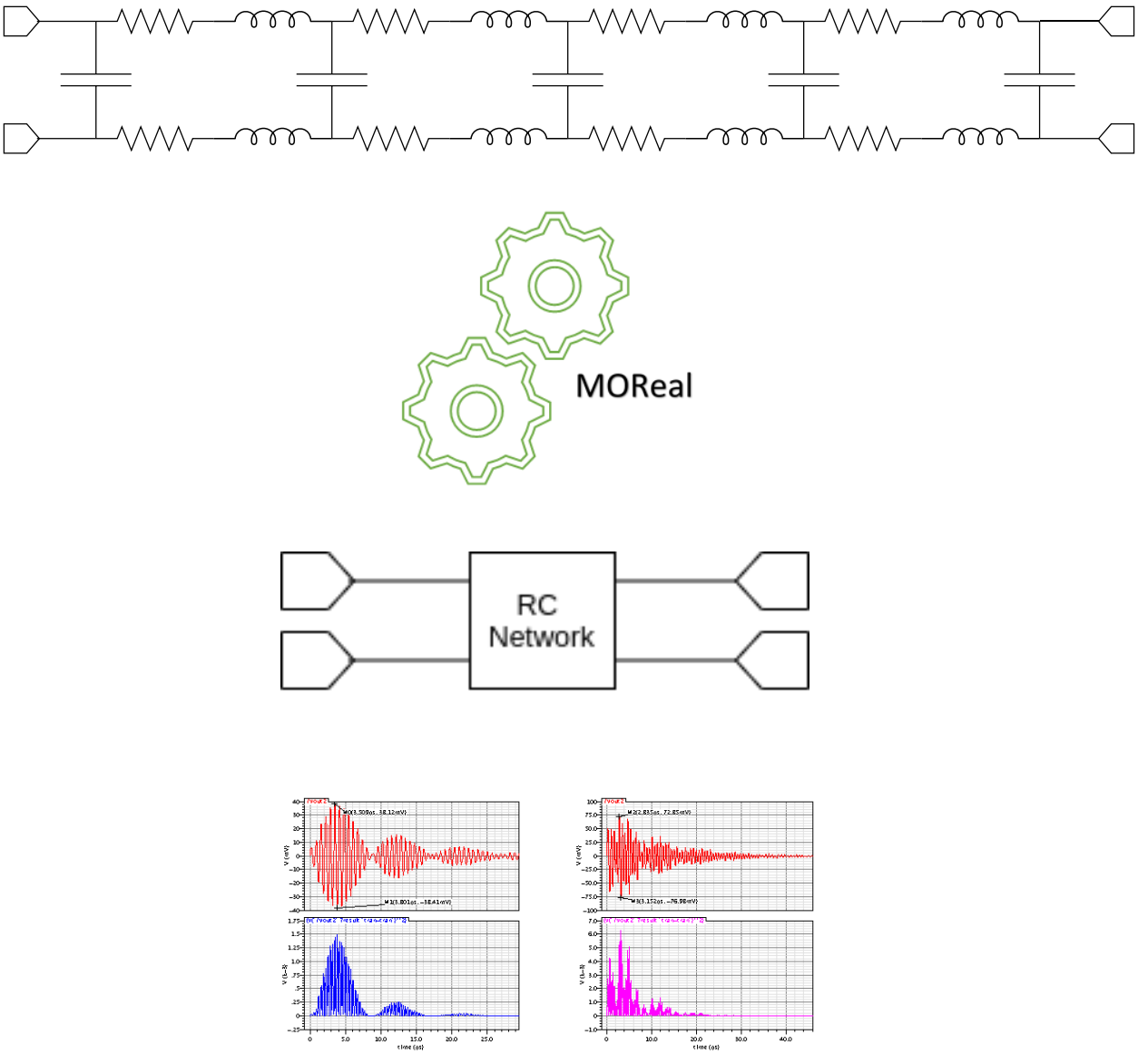

Figure 10 The graph illustrates How MOReal can reduce a massive RLCK circuit to an equivalent RC network.

Conclusion

MOReal can reduce large circuit rapidly to an equivalent small realizable circuit ready for simulation. Therefore, it is now possible for engineers to obtain realizable small circuits after extracting full electromagnetic parasitic netlists. MOReal's reduced circuits perform analyses and simulations very fast since they exhibit a small number of nodes and instances besides enhancing the mathematical conditioning of the systems.

Furthermore, MOReal's reduced netlists are guaranteed passive and numerically stable. MOReal can reduce analog and digital circuits so that engineers can implement MOReal in both analog and digital flows. To conclude, MOReal is the tool for timesaving to help engineers quickly finish their analyses or explore additional EM phenomena without worrying about time.